

signal (M_1) by approximately half a clock period of the external clock signal (C_0).

6. (Amended) A circuit arrangement as claimed in claim 1, characterized in that

- the first driver stage (40) comprises:
 - a clock signal input (42c) provided for the first clock signal (C_1);
 - a modulation signal input (42m) provided for the first modulation signal (M_1) for controlling the switching of each modulation voltage (U_{unmod} or U_{mod}) to the amplitude-modulated first power supply voltage ($U_{dd,1}$);
 - a first electronic switch (44);
 - a second electronic switch (46) arranged behind the first switch (44); and
 - an output (48) provided for the first output signal comprising the output voltage ($U_{o,1}$),
 - wherein the control means (442) of the first switch (44) and the control means (462) of the second switch (46) are each connected to the clock signal input (42c);
 - the power supply voltage-sided contact (444) of the first switch (44) is connected to the amplitude-modulated first power supply voltage ($U_{dd,1}$),

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- the reference potential-sided contact (464) of the second switch (46) is connected to the first reference potential ($U_{ss,1}$), and
- the output voltage-sided contact (446) of the first switch (44) and the output voltage-sided contact (466) of the second switch (46) are connected together and to the output (48), and
- in that the second driver stage (50) comprises:
 - a clock signal input (52c) provided for the second clock signal (C_2);
 - a modulation signal input (52m) provided for the second modulation signal (M_2) for controlling the switching of each modulation voltage (U_{unmod} or U_{mod}) to the amplitude-modulated second power supply voltage ($U_{dd,2}$);
 - a first electronic switch (54);
 - a second electronic switch (56) arranged behind the first switch (54); and
 - an output (58) provided for the second output signal comprising the output voltage ($U_{o,2}$),
 - wherein the control means (542) of the first switch (54) and the control means (562) of the second switch (56) are each connected to the clock signal input (52c),
 - the power supply voltage-sided contact (544) of the first switch (54) is connected to the

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- connected together and to the output (58).

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